I CLAIM:

1. A circuit for receiving a reference clock signal and outputting clock signals having different phases corresponding to said reference clock signal, said circuit comprising:

a plurality of serially-coupled delay units comprising a first delay unit operative to receive said reference clock signal, said plurality of serially-coupled delay units operative to output clock signals phase-shifted relative to said reference clock signal, each said delay unit of said plurality of serially-coupled delay units providing at least two stages of variable phase adjustment controllable by digital signals;

a phase detector operative to output a signal indicating a phase difference between said reference clock signal and a clock signal output by said plurality of serially-coupled delay units; and

logic circuitry operative to output digital signals to control phase shifts performed by said plurality of serially-coupled delay units based on said output of said phase detector.

2. The circuit of claim 1 wherein a delay unit of said plurality of serially-coupled delay units comprises:

at least one delay line comprising an input coupled to an input of said delay unit, said at least one delay line operative to output a first signal having a first phase and a second signal having a second phase; and

at least one phase mixer operative to receive said first and said second signals of said at

least one variable delay line, said at least one phase mixer operative to output a third signal having a third phase.

3. The circuit of claim 2 wherein said third phase is one of said first phase, said second phase or a phase in between said first and said second phases.

4. The circuit of claim 1 wherein said reference clock signal and said clock signals output by said plurality of serially-coupled delay units have substantially the same frequency.

5. The circuit of claim 1 wherein a delay unit of said plurality of serially-coupled delay units comprises at least one variable delay line.

6. The circuit of claim 5 wherein said at least one variable delay line comprises two variable delay lines.

7. The circuit of claim 1 wherein a delay unit of said plurality of serially-coupled delay units comprises at least one phase mixer.

8. The circuit of claim 1 wherein said at least two stages of phase adjustment comprises a coarse adjustment stage and a fine adjustment stage.

9. The circuit of claim 1 wherein said plurality of serially-coupled delay units outputs a corresponding plurality of output clock signals having different phases.

10. The circuit of claim 1 wherein said plurality of clock signals are phase-shifted by about (360/M)° to about 360° relative to said reference clock signal, where M is the number of delay units of said plurality of serially-coupled delays.

11. The circuit of claim 1 wherein said plurality of serially-coupled delay units are substantially identical to one another.

12. The circuit of claim 1 wherein said plurality of serially-coupled delay units are controlled by the same digital signals.

13. A circuit for receiving a reference clock signal and outputting clock signals having different phases corresponding to said reference clock signal, said circuit comprising:

a plurality of serially-coupled delay units comprising a first delay unit operative to receive said reference clock signal, said plurality of serially-coupled delay units operative to output clock signals phase-shifted relative to said reference clock signal, each said delay unit of said plurality of serially-coupled delay units providing at least two stages of digitally-controlled variable phase adjustment, wherein a delay unit of said plurality of serially-coupled delay units comprises:

two parallel delay lines each comprising an input coupled to an input of said delay unit, each said delay line operative to output a signal having a phase;

two parallel phase mixers each operative to receive said output signals from said two

parallel delay lines, said two phase mixers each operative to output a signal having a phase between said phases of said delay line output signals; and

a third phase mixer operative to receive said output signals from said two parallel phase mixers, said third phase mixer operative to output a third signal having a third phase;

a phase detector operative to output a signal indicating a phase difference between said reference clock signal and a clock signal output by said plurality of serially-coupled delay units; and

logic circuitry operative to digitally control phase shifts of said plurality of said serially-coupled delay units based on said output of said phase detector.

14. The circuit of claim 13 wherein said delay lines provide coarse phase adjustment.

15. The circuit of claim 13 where said two parallel phase mixers provide phase adjustment finer than said delay lines.

16. The circuit of claim 13 wherein said third phase mixer provides phase adjustment finer than said two parallel phase mixers.

17. A method of outputting clock signals having different phases corresponding to a reference clock signal, said method comprising:

receiving said reference clock signal;

generating a plurality of clock signals each phase-shifted differently relative to said reference clock signal;

measuring phase difference between said

reference clock signal and a clock signal of said plurality of clock signals; and

adjusting if necessary phase shifts of said plurality of clock signals digitally in at least two stages based on said measuring.

18. The method of claim 17 wherein said adjusting comprises adjusting said phase shifts by a first increment.

19. The method of claim 18 wherein said adjusting comprises adjusting said phase shifts by a second increment, said second increment smaller than said first increment.

20. A method of outputting clock signals having different phases corresponding to a reference clock signal, said method comprising:

receiving said reference clock signal;

generating a plurality of clock signals each phase-shifted differently relative to said reference clock signal;

measuring phase difference between said reference clock signal and a clock signal of said plurality of clock signals;

adjusting coarsely phase shifts of said plurality of clock signals in response to a measured phase shift; and

adjusting finely phase shifts of said plurality of clock signals in response to a measured phase shift.

21. The method of claim 20 further comprising adjusting more finely phase shifts of said plurality of clock signals.

22. Apparatus for outputting multi-phase clock signals corresponding to a reference clock signal, said circuit comprising:

means for receiving said reference clock signal;

means for outputting a plurality of clock signals phase-shifted relative to said reference clock signal, wherein said means for outputting said plurality of clock signals comprises means for providing a first stage of phase adjustment and a second stage of phase adjustment for each of said plurality of clock signals;

means for measuring phase difference between said reference clock signal and a clock signal of said plurality of clock signals; and

means for adjusting phase shifts of said plurality of clock signals based on measurements of said phase difference.

23. A computer system comprising:

a processor;

a memory controller coupled to said processor;

a plurality of dynamic random access memory (DRAM) chips coupled to said memory controller; and

circuitry for synchronizing with an external clock signal data output by said DRAM chips, said circuitry comprising:

circuitry for receiving said external clock signal;

circuitry for outputting a plurality of clock signals phase-shifted relative to

said external clock signal, wherein said circuitry for outputting said plurality of clock signals comprises circuitry for providing a first stage of phase adjustment and a second stage of phase adjustment for each of said plurality of clock signals;

circuitry for measuring phase difference between said external clock signal and a clock signal of said plurality of clock signals; and

circuitry for adjusting phase shifts of said plurality of clock signals based on measured said phase differences.